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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	19

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application	Applicant(s)	
	09/886,368	HAMAMOTO ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *55-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *55-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on February 10, 2004. Claim 57 was amended. Claims 61-72 were added. Claims 55-72 of the application are pending. This office action is made final.

Response to Amendments

2. Applicants' arguments, filed on February 10, 2004 have been fully considered. Applicant's arguments, filed on February 10, 2004 under 35 U.S.C. 103 (a) are not persuasive. Examiner's response to the applicants' arguments is presented in Paragraph 10 below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

4. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 55, 60, 61, 66, 67 and 72 are rejected under 35 U.S.C. 103(a) as being over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Welsh et al. (WE)** (U.S. Patent 4,955,070).

5.1 **KKR** teaches portable data processing and storage system. Specifically, as per Claim 55, 61 and 67, **KKR** teaches a digital signal source (Col 2, Lines 19-21; Col 6, L24-28);

a (plurality of) memory apparatus having a playback function removably connected with a digital signal source to store digital data received from the digital signal source (Col 1, Line 61 to Col 2, Line 24; Col 4, Lines 6-8; Col 6, Lines 24-28); and

to reproduce the digital data stored therein independently of the digital signal source (Col 1, Line 61 to Col 2, Line 24); comprising:

a memory circuit electrically connected for storing said digital data from the digital signal source (Col 1, Line 61 to Col 2, Line 24; Col 2, Lines 45-53; Col 6, Lines 24-30 & 44-49); and

a playback circuit for reproducing said digital data stored in said memory circuit (Col 1, Line 61 to Col 2, Line 24).

KKR does not expressly teach that the memory apparatus has an inner battery. **WE** teaches that the memory apparatus has an inner battery (Col 2, Lines 3-7; Fig.6, Item 162; Col 6, Lines 20-24), as the battery allows portable use of the memory apparatus (Col 2, Lines 3-7). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with inner battery of **WE**, as the battery would allow portable use of the memory apparatus.

KKR does not expressly teach a battery switch, wherein the battery switch enables to use power from the digital signal source having a higher operating voltage than that of the inner battery when the memory circuit stores the digital data in a condition of connecting to the digital signal source. **WE** teaches a battery switch, wherein the battery switch enables to use power from the digital signal source when the memory circuit stores (transfers) the digital data in a condition of connecting to the digital signal source (Fig. 1, Items 30 and 12; Fig. 6, switch between the battery charger and the power conditioning circuit; Fig. 8, Item 185; Col 6, Lines 20-26; Col 6, Lines 33-35; Col 7, Lines 21-29: the electronically controlled switch is one or more solid state devices and may be located in the power supply), as the battery switch allows operation of the portable unit from the power from the battery charger circuit (Fig 6, Item 164) when the onboard power supply unit (Fig 1, Item 30) is connected to the base unit (Fig 1, Item 12) and operate the portable unit from the battery (Fig 6, Item 162) when the battery charger circuit (Fig 6, Item 164) is disconnected from the base unit (Fig 1, Item 12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention

to modify the memory apparatus of **KKR** with the apparatus of **WE** that included a battery switch, wherein the battery switch enabled to use power from the digital signal source when the memory circuit stored (transferred) the digital data in a condition of connecting to the digital signal source, as the battery switch would allow operation of the portable unit from the power from the battery charger circuit when the onboard power supply unit was connected to the base unit and operate the portable unit from the battery when the battery charger circuit was disconnected from the base unit.

KKR does not expressly teach a power switch, wherein the power switch enables the memory apparatus to use interconnected higher voltage power from the digital signal source in comparison to the voltage level of the inner battery during times when the memory circuit stores the digital data while connected to the digital signal source. **WE** teaches a power switch, wherein the power switch enables the memory apparatus to use interconnected power from the digital signal source during times when the memory circuit stores (transfers) the digital data while connected to the digital signal source (Fig. 1, Items 30 and 12; Fig. 6, switch between the battery charger and the power conditioning circuit; Fig. 8, Item 185; Col 6, Lines 20-26; Col 6, Lines 33-35; Col 7, Lines 21-29: the electronically controlled switch is one or more solid state devices and may be located in the power supply), as the power switch allows operation of the portable unit from the power from the battery charger circuit (Fig 6, Item 164) when the onboard power supply unit (Fig 1, Item 30) is connected to the base unit (Fig 1, Item 12) and operate the portable unit from the battery (Fig 6, Item 162) when the battery charger circuit (Fig 6, Item 164) is disconnected from the base unit (Fig 1, Item 12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify

the memory apparatus of **KKR** with the apparatus of **WE** that included a power switch, wherein the power switch enabled the memory apparatus to use interconnected power from the digital signal source during times when the memory circuit stored (transferred) the digital data while connected to the digital signal source, as the power switch would allow operation of the portable unit from the power from the battery charger circuit when the onboard power supply unit was connected to the base unit and operated the portable unit from the battery when the battery charger circuit was disconnected from the base unit.

KKR and **WE** does not expressly teach the digital signal source having a higher operating voltage than that of the inner battery; and having higher voltage power in the digital signal source in comparison to the voltage level of the inner battery. It is inherent and one of ordinary skill in the art knows that the digital signal source has higher operating voltage than that of the battery, because the current can flow from the digital signal source to the battery for charging only when the digital signal source has higher voltage than that of the battery. The current flow is a function of the voltage differential and the resistance of the charging circuit and the battery. (The applicants' attention is directed to Paragraph 10.1 for a reference provided as per the applicants' request.)

KKR does not expressly teach a battery switch to use power from the inner battery when the playback circuit reproduces the digital data in a condition of being removed from the digital signal source. **WE** teaches a battery switch to use power from the inner battery when the playback circuit reproduces the digital data in a condition of being removed from the digital source (Fig. 6, Item 162; Fig. 8, Item 185; Col 7, Lines 21-29: the electronically controlled switch is one or more solid state devices and may be

located in the power supply), as the inner battery allows portable use of the memory apparatus (Col 2, Lines 3-7). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the apparatus of **WE** that included a battery switch to use power from the inner battery when the playback circuit reproduced the digital data in a condition of being removed from the digital signal source, as the battery would allow portable use of the memory apparatus.

KKR does not expressly teach a power switch to use power from the inner battery when the playback circuit reproduces the digital data when the memory apparatus is detached from the digital signal source. **WE** teaches a power switch to use power from the inner battery when the playback circuit reproduces the digital data when the memory apparatus is detached from the digital signal source (Fig. 6, Item 162; Fig. 8, Item 185; Col 7, Lines 21-29: the electronically controlled switch is one or more solid state devices and may be located in the power supply), as the inner battery allows portable use of the memory apparatus (Col 2, Lines 3-7). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the apparatus of **WE** that included a power switch to use power from the inner battery when the playback circuit reproduced the digital data when the memory apparatus was detached from the digital signal source, as the battery would allow portable use of the memory apparatus.

5.2 As per Claims 60, 66 and 72, **KKR** and **WE** teach the memory apparatus of claim 55. **KKR** also teaches that the memory apparatus is a personal audio player for playing

vended audio programs, and wherein the digital source is an audio program vending machine (Col 1, Line 64 to Col 2, Line 24; Col 6, Lines 24-30 and Lines 44-49).

6. Claims 56, 62 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Welsh et al. (WE)** (U.S. Patent 4,955,070), and further in view of **Jinguji (JI)** (U.S. Patent 4,847,840).

6.1 As per Claims 56, 62 and 68, **KKR** and **WE** teach the memory apparatus of claims 55 and 61 and the digital signal source of claim 67. **KKR** does not expressly teach that the digital data includes audio data and an identification (ID) code specifying a reproducing condition of the audio data, and the playback circuit reproduces the audio data following the reproducing condition. **JI** teaches that the digital data includes audio data and an identification (ID) code specifying a reproducing condition of the audio data, and the playback circuit reproduces the audio data following the reproducing condition (Col 12, Lines 63-67; Col 12, Lines 47-49), as the identification data indicate if the audio data is monaural or stereo data and the sampling frequency to be used (Col 12, Lines 63 to Col 13, Line 16). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the memory apparatus of **JI** that included the digital data including audio data and an identification (ID) code specifying a reproducing condition of the audio data, and the playback circuit reproduced the audio data following the reproducing condition, as the identification data would indicate if the audio data was monaural or stereo data and the sampling frequency to be used.

7. Claims 57, 63 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Welsh et al. (WE)** (U.S. Patent 4,955,070) and **Jinguji (JI)** (U.S. Patent 4,847,840), and further in view of **Koguchi et al. (KOG)** (U.S. Patent 5,138,925).

7.1 As per Claims 57, 63 and 69, **KKR, WE** and **JI** teach the memory apparatus of the memory apparatus of claims 56 and 62 and the digital signal source of claim 68. **KKR** and **WE** do not expressly teach that the ID code is inserted in the head of the digital data and is followed by the audio data, and the ID code and the audio data are integrally stored in the memory circuit. **KOG** teaches that the ID code is inserted in the head of the digital data and is followed by the audio data, and the ID code and the audio data are integrally stored in the memory circuit (Col 7, Lines 24-28; Col 7, Lines 41-47; Col 11, Lines 25-26; Col 12, Lines 28-29; Col 21, Lines 11-12), as the ID code indicates the type of message (Col 11, Lines 25-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** and **WE** with the memory apparatus of **KOG** that included the digital data including audio data and an identification (ID) code specifying a reproducing condition of the audio data, and the playback circuit reproduced the audio data following the reproducing condition, as the ID code would indicate the type of message.

8. Claims 58, 64 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Welsh et al. (WE)** (U.S. Patent 4,955,070), and further in view of **Etoh et al. (ET)** (U.S. Patent 5,297,097).

8.1 As per Claims 58, 64 and 70, **KKR** and **WE** teach the memory apparatus of claims 55 and 61 and the digital signal source of claim 67. **KKR** and **WE** do not expressly teach a data transfer circuit to operate at an increased data transfer speed at the higher operating voltage from the digital source, in comparison to a data transfer speed at an operating voltage of the inner battery. **ET** teaches a data transfer circuit to operate at an increased data transfer speed at the higher operating voltage from the digital source, in comparison to a data transfer speed at an operating voltage of the inner battery (Fig. 1C; Col 2, Lines 47-57; Col 5, Lines 7- 17; Col 8, Lines 6-29), as the performance of the system is greatly improved with higher voltage (Fig. 1C; Col 8, Lines 24-29). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** and **WE** with the memory apparatus of **ET** that included a data transfer circuit to operate at an increased data transfer speed at the higher operating voltage from the digital source, in comparison to a data transfer speed at an operating voltage of the inner battery, as the performance of the system would be greatly improved with higher voltage.

9. Claims 59, 65 and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Welsh et al. (WE)** (U.S. Patent 4,955,070), and further in view of **Koenck (KO)** (U.S. Patent 4,737,702).

9.1 As per Claims 59, 65 and 71, **KKR** and **WE** teach the memory apparatus of claims 55 and 61 and the digital signal source of claim 67. **KKR** does not expressly teach that the inner battery is a rechargeable battery. **WE** teaches that the inner battery is a rechargeable battery (Col 2, Lines 3-7; Fig.6, Item 162), as the rechargeable battery allows portable use of the memory apparatus (Col 2, Lines 3-7); and as per **KO**, the rechargeable battery provides increased useful life and reliability (Col 1, Lines 52-53). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the memory apparatus of **WE** that included a rechargeable battery, as the rechargeable battery would allow portable use of the memory apparatus and as per **KO**, the rechargeable battery would provide increased useful life and reliability.

KKR does not expressly teach the memory apparatus comprises a recharge circuit to use the higher operating voltage from the digital signal source to rapidly recharge the rechargeable battery during data transfer from the digital signal source to the memory apparatus. **WE** teaches the memory apparatus comprises a recharge circuit to use the higher operating voltage from the digital signal source to rapidly recharge the rechargeable battery during data transfer from the digital signal source to the memory apparatus (Fig. 1, Items 30; Fig. 6, Item 164; Col 6, Lines 20-26), as the battery charger circuit (Fig 6, Item 164) allows the rechargeable battery to be recharged (Col 6, Lines 20-23) when the onboard power supply unit (Fig 1, Item 30) is connected to the base unit (Fig 1, Item 12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the apparatus of

WE that included the memory apparatus comprising a recharge circuit to use the higher operating voltage from the digital signal source to rapidly recharge the rechargeable battery during data transfer from the digital signal source to the memory apparatus, as the battery charger circuit would allow the rechargeable battery to be recharged when the onboard power supply unit was connected to the base unit .

Arguments

10. Examiner's response to the Applicants' arguments re presented below.

10.1 As per the applicants' argument that "the statement made by apparent judicial (Examiner) notice in the Office Action in support of art rejections to assert that certain claimed features are well known in the art; the Examiner should cite a reference which factually supports his position or withdraw such assertions", the examiner has provided a reference, **Chandler (CH)** (U.S. Patent 3,660,714, Issued date of May 1972).

CH teaches the digital signal source having a higher operating voltage than that of the inner battery; and having higher voltage power in the digital signal source in comparison to the voltage level of the inner battery (Col 3, Lines 47-54), as higher voltage above that of the battery is required at the digital signal source for the battery to be charged (Col 3, Lines 47-54).

10.2 As per the applicants' argument that "Applicants' battery switch enables use of higher operating voltage power from the digital signal source (in comparison to the lower

voltage level of the apparatus' internal rechargeable battery) during times when the memory circuit stores (i.e. downloads) the digital data while connected to the digital signal source; ... Welsh et al., at best, only vaguely discusses that battery 162 (Fig 6) may be a 6 volt battery and that the base unit preferably has a connection to conventional household AC electrical power at terminals 38, 40; Nowhere does Welsh et al. discuss what type of voltage is provided through the monitor/base direct electrical connections 32 and 34; it seems that 6 volts is the most likely candidate, since to allow AC electrical power to be applied across connections 32, 34 would destroy the monitor's circuitry and/or blow up the battery", the examiner has taken the position that it is inherent and one of ordinary skill in the art knows that the digital signal source has higher operating voltage than that of the battery for the current to flow from the digital signal source to the battery for charging. The Examiner has also provided a reference (**CH:** Col 3, Lines 47-54), which teaches that higher voltage is needed at the digital signal and power source for the battery to be charged.

The examiner also directs the applicants' attention to the fact that the on-board power supply unit in Welsh et al. has a power conditioning circuit (Fig 6, Item 166), which provides various levels of voltage to the circuitry as needed (Col 6, Lines 25-26); the base unit (Fig 7) has a similar power conditioning circuit (Item 172) to provide appropriate voltage power at terminals 32-34 (Col 6, Lines 33-35); the applicants' assertion that "it seems that 6 volts is the most likely candidate, since to allow AC electrical power to be applied across connections 32, 34 would destroy the monitor's circuitry and/or blow up the battery" is incorrect.

10.3 As per the applicants' argument that "Welsh et al.'s Fig 6 has only a diode between its battery charger and the power conditioning circuit", the examiner takes the position that the Application shows only a diode 1201 on Figure 12 between the terminal device and the memory circuit 701 and the specification discusses only a diode on Page 35, Line 13 to Page 36, Line 15. Therefore, the Applicants' claimed battery switch/power switch is nothing more than a diode. The Examiner has indicated that Welsh et al. teaches and suggests an electronically controlled battery switch/power switch in the power supply unit (Col 7, Lines 21-29; Fig. 8, Item 185).

10.4 As per the Applicants' request for an Examiner interview, the Examiner takes the position that the Applicants' claims are neither novel nor non-obvious and therefore no useful purpose will be served by such an interview. Therefore, the Applicants' request for interview is not deemed necessary at this time.

Conclusion

ACTION IS FINAL

11. Applicant's arguments with respect to claim rejections under 35 USC § 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
April 20, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER